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Review
Silicon solar cells for terrestrial applications

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The ways in which silicon solar cells can be designed to give maximum efficiency are reviewed. It is suggested that, although the reduction of processing costs is an extremely important objective of the development programme aimed at widespread application in highly developed countries, the improvement of design might have sufficient cost benefit even if based on current processing technology for the application of solar cells in remote localities which are not easily served with electricity via transmission lines.

1. Introduction

As early as 1958, silicon diffused p–n junctions were being made commerically for use in photometry and other light-sensing applications. Even at this early stage, 14% efficiency was obtainable, and all that was needed to stimulate further development was a market. This requirement was met when the Russians successfully demonstrated that solar power was the ideal source of energy for space applications [1].

For these applications, the emphasis was placed on producing cells resistant to damage caused by energetic radiation and to temperature cycling, having high reliability and low power to weight ratios. Only the silicon solar cell proved adaptable to meet these requirements, and its rivals were soon eliminated: GaAs because of its high surface absorption and consequently low collection efficiency (despite its high quantum efficiency), and CdS because of its unreliability and low efficiency (despite its low cost and high resistance to radiation-induced damage).

With the growing interest in using solar generation of power on earth, and with the rapid advance in the technology of devices based on GaAs, CdS, and other materials, it becomes necessary to re-examine silicon solar cells and to predict whether they can compete in the low-cost solar cell market. Many developing countries in areas of abundant sunshine will provide a large market for solar cells, and it is misleading to lay too much stress on the stringent low-cost requirement needed for adequate US consumption.

This paper is intended to bring together all the advances which have been made in the production and design of solar cells, particularly silicon diffused junctions, and to qualitatively discuss the economics of their application outside the US. It is hoped that this will lead to more detailed consideration of the developments needed to produce cells useful in these applications.

2. The economics of solar cells

It has been estimated recently that the materials cost target for acceptably low-cost solar cells is about 25 cents/watt [2] for silicon devices. Of course this applies to cells produced for the American market, the aim being to supply about 1% of the US electricity by photovoltaic conversion of sunlight by 1990–2000. This very low materials price arises because the materials component is the largest contribution to the installation cost, and solar cell installations must be able to produce electricity cost-competitively with nuclear and conventional generators of the type already used, or being developed.

In countries outside the US, particularly in the developing countries of the Middle East, Asia and Africa, the economics of solar cell utilization are very different from those which apply in the US. First, these countries do not already have the technology needed to build conventional and nuclear generators, so that these have to be imported, with the obvious economic and political disadvantages entailed in this. Secondly, outside a few major cities in each country, the major demand comes from small isolated communities distributed over wide areas. The essential requirements here are for small output, highly reliable installations having low capital cost, and for a means of cheap distribution. Clearly, solar cells provide a very suitable means of meeting these requirements; as sunshine is already distributed, the maintenance of photovoltaic installations is minimal and the installations can be economically operated on a small scale. The main problem is the efficient storage of the solar-generated power, but once this is solved, photovoltaic cells should find widespread application for electricity generation in rural communities and for powering repeater stations in the telecommunications links across sparcely populated areas.

It is by no means clear what the exact size and cost-requirement of this market will be, but it is probable that the cost of cells will have to be reduced below that of those used on spacecraft. It is also likely that a cost above the figures quoted for economic use of solar cells in the US could be tolerated, when it is considered that American users tend to be concentrated in large communities, the distribution networks already exist, and the capital invested to date in conventional electricity generation is substantial.

There are four ways that solar cell utilization can be made more economical:

(a) by developing current technology in a way which will allow cheaper processing;

(b) by designing improved efficiency cells which can be manufactured without too much increase in cost;

(c) by using concentrated radiation to increase the output per unit area of solar cell;

(d) by using new, cheaper production technologies, with a tolerable reduction in device efficiency.

In order to meet the requirements of the American market (a reduction in cost by two orders of magnitude), only the last approach shows promise. However, this should not divert effort completely from the other possibilities, because of the needs of countries outside the US.

The most widely used solar cell to date has been the silicon diffused p–n junction type. In the following sections, the mode of operation and the efficiency for such devices will be discussed, with emphasis on why silicon is preferred, and how the cell design can be optimized. This is followed by a discussion of the photovoltaic conversion of concentrated radiation, and finally, methods of producing solar cells are reviewed, stressing areas in which the research scientist rather than the development still has a part to play.

3. Efficiency of a homojunction device

These devices rely on the photogeneration of electron-hole pairs in a semiconductor, and their separation at a potential discontinuity, so that electrical power can be extracted. We deal here with silicon devices in which this discontinuity is provided by a diffused p–n junction. The theory of operation of such devices has been recently reviewed [3, 4] but since a fundamental picture of how the devices operates is necessary to subsequent discussion in this paper, such a picture is presented here.

The physics of silicon p–n junction diodes is well known. The operation of such a device as a solar cell is essentially different from that of a diode in that the deviation from thermal equilibrium, necessary to produce a nett conversion of energy by the device, is achieved by using incident radiation rather than by applying a voltage. Specifically, the light has two effects:

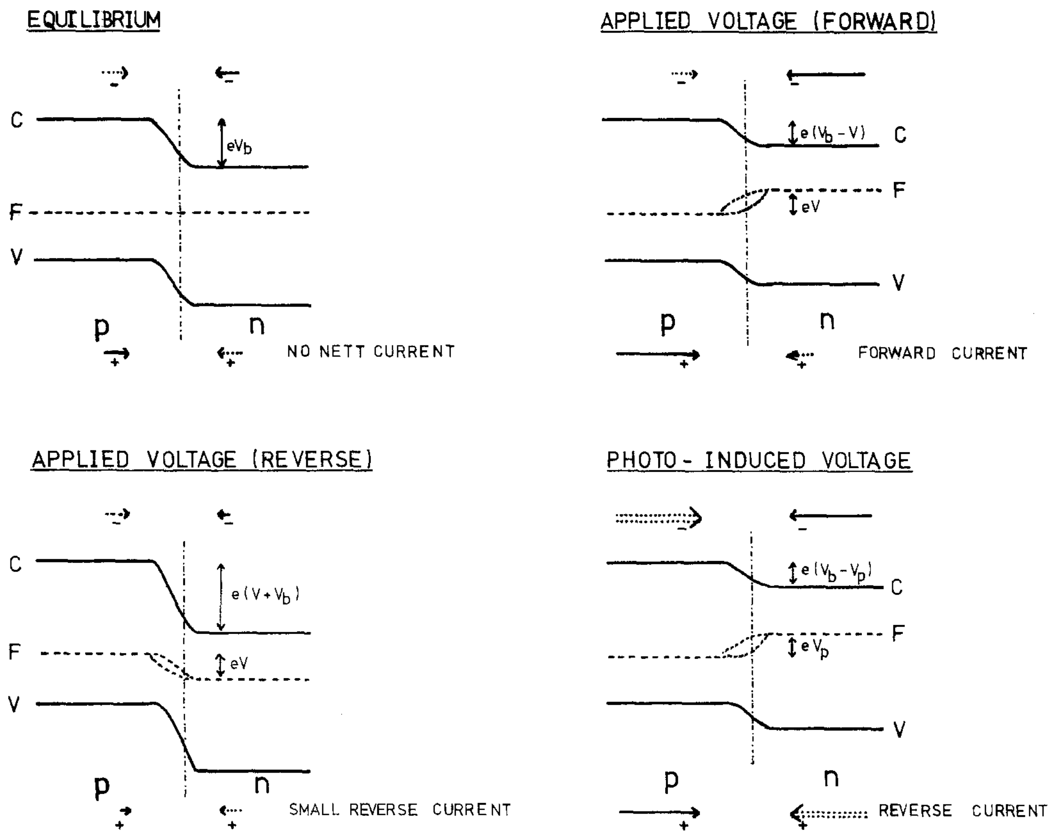
(a) the current of minority carriers crossing the junction (to become majority carriers) is increased;

(b) the height of the potential barrier at the junction is reduced by this current, to an extent determined by the load resistance.

This reduction in barrier height is analogous with the effect of a forward bias on the cell, so that light is said to produce a photovoltage. However, the current of majority carriers which can cross the barrier because of its reduced height is not useful in photovoltaic generation because it opposes the flow of light-generated minority carriers. Thus the normal diode equation can be modified to describe the operation of a photovoltaic cell:

$$-J = J_L - J_R - J_o\left[\exp\left(\frac{eV_p}{kT}\right)^{-1}\right] \qquad (1)$$

where J_L is the rate of generation of minority carriers per unit volume in the device, J_R is the volume rate of their recombination, V_p is the photovoltage, k is Boltzmann's constant, T is temperature and J_0 is the diode saturation current.


EQUILIBRIUM

APPLIED VOLTAGE (FORWARD)

APPLIED VOLTAGE (REVERSE)

PHOTO - INDUCED VOLTAGE

Figure 1 Operation of a p–n junction. $\dashrightarrow$ minority carriers; $\overset{-}{\dashrightarrow}$ electrons; $\overset{+}{\dashrightarrow}$ holes. $\longrightarrow$ majority carriers; $\overset{-}{\longrightarrow}$ electrons; $\overset{+}{\longrightarrow}$ holes. The length of the arrow indicates the size of the current, although not to scale. C = conduction band edge, F = Fermi level, V = valence band edge.

Fig. 1 shows the way in which the device works as (a) a diode and (b) a photovoltaic converter. The minority carrier current in the latter case increases as the illumination level increases, or, at constant illumination level, as the load resistance decreases. The photovoltage at constant illumination level, however, decreases as the load resistance decreases, so the power delivered by the device is maximum at some intermediate load.

We can now describe the factors which are used to compare the overall efficiency of photovoltaic devices:

(1) the quantum efficiency, $J_{\mathrm{ph}}:J_{\mathrm{L}}$, where J_{ph} is the incident photon flux. This describes the efficiency of photon absorption;

(2) the voltage factor $eV_{\mathrm{oc}}:E_{\mathrm{g}}$, where V_{oc} is the photovoltage at a given light intensity with infinite load resistance, and E_{g} is the material (usually silicon) bandgap. This factor essentially describes the efficiency of energy conversion from absorbed photons;

(3) the current factor $J_{\mathrm{sc}}:J_{\mathrm{L}}$ where J_{sc} is the current flowing for a given illumination level, at zero load resistance. This factor describes the efficiency of carrier collection;

(4) the power factor $A:J_{\mathrm{sc}}V_{\mathrm{oc}}$, where A is the area under the $J-V$ curve for the device, at constant illumination level, bounded by the $J=0$ and $V=0$ axes. The shape of the $J-V$ curve (for given J_{sc} and V_{oc} and given illumination level) is determined by the series resistance in the circuit (i.e. the load resistance and the device internal resistance), and this ratio (often called the fill factor) describes the efficiency of power extraction.

We can only quantitatively define the efficiency of the cell for a single illumination level, temperature and spectral distribution of incident light. Note that the spectral distribution in sunlight is changed by atmospheric absorption, so that precise conditions have to be stated in any determination of cell efficiency in sunlight.

From these considerations, we see that the device should have low reflection losses for light (high quantum efficiency), large values of V_{oc} and J_{sc} and low series resistance. We can simplify Equation 1 by assuming that $J_L \gg J_o$ and J_R. Thus, at open circuit ($V_p = V_{oc}$);

$$V_{oc} = \frac{kT}{e} \ln\left(\frac{J_L}{J_o}\right). \qquad (2)$$

Thus the open circuit voltage can be increased by reducing J_o, and hence the current of majority carriers leaking across the junction during operation.

We can now discuss the ways in which these criteria are met in practice.

4. Physical factors which determine homojunction solar cell efficiencies

There are four distinct types of variables which determine the overall performance of a solar cell of this type:

(1) properties intrinsic to the material chosen;
(2) extrinsic materials properties;
(3) the cell design;
(4) the mode of operation.

Several reviews have been published which deal with these in detail (see, for example, [5–8]) and no exhaustive treatment is needed here. Instead, a descriptive picture is given of the contribution each of the factors listed makes to the cell efficiency achieved.

4.1. Intrinsic materials properties

4.1.1. Bandgap

Photons of energy $h\nu < E_g$ cannot excite band-to-band transitions, and are thus not useful in photovoltaic generation. Photons of energy $h\nu > E_g$ excite electrons into states some way above the conduction band edge and their relaxation to the band edge constitutes a loss of useful energy. Thus, the solar spectrum is absorbed usefully to an extent determined by E_g. On the basis of these considerations, the optimum bandgap for solar absorption is about 1.1 eV.

However, maximum useful absorption does not necessarily correspond to maximum power delivered, because the leakage current, and hence the open circuit voltage, is also dependent upon bandgap. Majority carrier leakage increases exponentially as the band gap is reduced, and the optimum bandgap for maximum power output at room temperature is about 1.5 eV [9].

The majority carrier leakage current also depends exponentially upon temperature, so that the optimum bandgap for maximum power output increases with temperature, and the actual maximum power obtainable decreases [10]. In effect, a loss of efficiency due to reduced photon absorption must be tolerated in order to increase V_{oc}. Thus, at room temperature the maximum theoretical efficiency is about 28% for a bandgap of 1.5 eV, while at 300° C, it is reduced to about 11%, and corresponds to a 1.8 eV bandgap.

4.1.2. Transition type

Direct-gap materials absorb photons more efficiently than indirect-gap materials, since they are characterized by fast band-to-band excitation of electrons, without the need for phonon interaction. For precisely the same reason, direct gap materials are subject to fast radiative recombination processes. Thus devices based on direct gap materials can be very thin (absorption is complete within about 5 μm), and for the same reason can be polycrystalline provided that the grain size exceeds about 5 μm. However recombination losses tend to be high, because the absorption region is coincident with the defective surface region of the cell, and because band-to-band recombination in the bulk is fast. Bulk recombination is not very important in a 5 μm thick device, because the actual distance over which carriers must diffuse if they are to be separated by the junction field is relatively small, so that a fairly high recombination velocity can be tolerated. Surface recombination is, however, a much more serious problem.

Indirect-gap materials show a non-abrupt absorption edge, so that the depth of penetration of photons into the material depends upon their wavelength [11, 12]. In these materials, the blue response is limited by surface recombination and the red response primarily by the diffusion length of minority carriers in the base region [13]. The total active depth of an indirect gap material is typically about 100 μm and in all but the most perfect material, the red response is limited by the fact that the corresponding minority carriers generated recombine without reaching the junction. The actual spectral response of the cell depends upon the distribution of electric field within it [14] and we shall see later how considerations based on this absorption

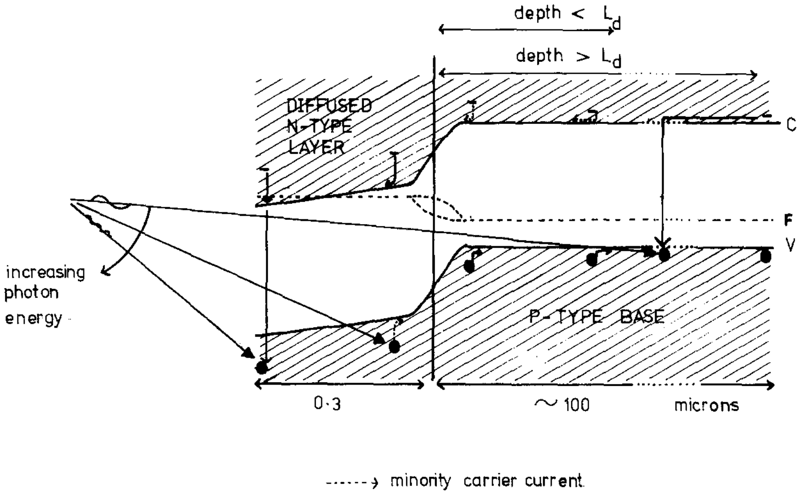


Figure 2 Spectral response of a diffused n-on-p cell: L_d = diffusion length in the base. • = represents holes; – represents electrons. C = conduction band edge, F = Fermi level, V = valence band edge.

behaviour affect the design of silicon cells. Fig. 2 shows a typical band scheme for absorption in a silicon cell.

4.1.3. Materials for solar cells

Silicon is not, in theory, the best solar cell material, because its band gap (1.1 eV) is below the optimum, even at room temperatures. Its theoretical efficiency is about 25% at 25° C, falling to about 2% at 300° C. Also, since it is an indirect-gap material, it cannot be used in thin film form to make devices. Three extensive reviews on the use of other materials have appeared recently [8, 15 16] and no attempt is made here to cover the possibilities in depth. Instead the important points of comparison are indicated.

GaAs has a bandgap of 1.4 eV, and is therefore, in theory, more efficient than silicon, particularly at high temperatures. It has a sharp absorption edge, as expected, since it is a direct-gap material and it is this factor which limits its practical use. New technological developments which allow graded III–V structures to be produced offer the possibility of using large band-gap windows so that high energy photons are transmitted through the window and absorbed away from the crystal surface. Such techniques are expensive in production, but they can be used to give photovoltaic efficiencies approaching the maximum predicted theoretically. The use of concentrated radiation to reduce cost by increasing the power output per unit area is attractive for GaAs because the material can withstand the associated rise in operating temperature. However, although high efficiency devices can be made economically, it is by no means clear that the necessary concentrator system can be made cheaply, or that such systems will be able to show long-term reliability [17].

The other serious contender to silicon is the CdS:Cu_2S heterojunction. Although CdS has a very large band-gap (~2.4 eV) its photovoltaic response, and the variation of this response with temperature, are characteristic of the theoretical behaviour of a material of band-gap 0.8 to 1.0 ev [9], probably because of the presence of localized energy levels within the forbidden gap. The main advantage of this material is that its photovoltaic properties are not substantially changed by its crystalline perfection, and evaporated films show behaviour very similar to that of the bulk crystals (this is characteristic of direct gap materials). This offers the possibility of cheap, large area devices. Control over the stoichiometry of both the CdS and the Cu_2S is, however, essential if degradation of the devices is to be avoided, and this might increase the cost of production. Also, the complex optical and electrical properties of CdS are not fully understood, so that optimising the design of the cells must rely on a semi-empirical approach, which can involve lengthy development.

Other heterojunction devices are being tried as solar cells, but these are not yet past initial stages of development. Silicon has powerful advantages to offer: it is an abundant material, and the techniques for processing it are very highly developed.

Despite this, extensive work is needed before silicon solar cells provide the answer for low-cost, terrestrial solar energy conversion.

4.2. Extrinsic materials properties

4.2.1. Doping

We have seen that large band gap materials are characterized by low majority carrier leakage across the junction. This current is determined by the height of the potential barrier at the junction, decreasing exponentially as the barrier height increases. For a given material band-gap, the barrier height is increased as the Fermi level approaches the conduction band edge in the n-type material and the valence band edge in the p-type material. Thus, increased doping on both sides of the junction decreases J_o and hence increases V_{oc}. The power delivered to a load also increases with increased doping because of the reduced cell resistance.

However, experimental curves of power output versus doping level show a maximum. If the doping is too high, J_R increases because of the corresponding decrease in minority carrier lifetime and mobility (note, however, that for silicon, the maximum impurity content tolerable is about 10^3 greater than for most other electronic applications [6]). At still higher doping levels, the open circuit voltage also starts to fall off, because of the influence of impurity band formation on the leakage current. A theoretical analysis of the effect of doping on solar cell efficiency has been presented by Dunbar and Hauser [18].

In practice, the optimum doping level for maximum efficiency is very dependent on the other extrinsic properties which determine the minority carrier diffusion length, and the defect content of the material is particularly important in this respect [19].

4.2.2. Crystal quality

Defects and unwanted impurities in a crystal introduce trapping levels into the forbidden gap which reduce the minority carrier lifetime and mobility in the material. In general, elemental semiconductors can be made much more perfect than compound materials, because the latter almost always have a finite compositional existence region, and hence a fairly high vacancy content. Silicon can be produced in a highly perfect state, so that the long minority diffusion lengths required due to its indirect-gap characteristics can be achieved, given sophisticated processing for materials preparation. A systematic study of the effect of base-region perfection on minority carrier lifetime, and hence on short-circuit current, has recently been published [20], showing that the short circuit current of the device falls off rapidly when the diffusion length for minority carriers in the base region is reduced below the base width.

We have already seen that the blue response of the silicon cell is determined primarily by the surface recombination velocity, so that surface perfection is particularly important. The red response is likely to be determined by the crystalline quality (and doping level) of the base region.

Defects in the junction region of the device are particularly harmful since they can increase recombination losses, and more importantly they enhance the thermal excitation of majority carriers across the junction (via the traps) thus increasing J_o and reducing V_{oc}. (Non-abruptness of the junction profile has a similar effect on V_{oc}). Junction imperfections are primarily responsible for the non-ideal open circuit voltage observed in diffused silicon cells [18] and high doping levels only improve the performance of devices in practice when the junction quality is very good.

Recently, there has been a good deal of interest in using polycrystalline silicon in solar cells, so that the role played by grain boundaries in solar cell performance is becoming important. These boundaries act as sinks for impurity atoms [21, 22] and also are characterized by a high defect density which can cause enhanced recombination [22, 23]. The relative importance of the two processes has yet to be established, but a model based on the first mechanism [22] has allowed the resistance of polycrystalline silicon to be derived as a function of its dopant level, in good agreement with experiment. The superiority of epitaxially grown junctions over diffused junctions [24] on polycrystalline material also favours the first mechanism of performance degradation, since preferential grain boundary diffusion is expected to enhance the effect. Polycrystalline material of grain size 100 μm to 1 mm has been used to fabricate devices having acceptable efficiency (for example, [24]), but much more experimental and analytical work is needed to determine the minimum grain size acceptable.

4.3. Design for diffused junction cells

A solar cell must be designed with the following requirements in mind: optimum spectral response; minimized series resistance; maximized collection efficiency; maximized heat dissipation; optimized base resistance; optimized base width. The way in which these requirements are met for diffused silicon solar cells are considered in the following sections and alternatives to the diffused junction, which might allow better designs to be used, are discussed later.

4.3.1. Spectral response

It is clear from Fig. 2, and from [14] and [25], that the spectral response of a cell having given minority carrier recombination rates in (a) the surface, (b) the diffused layer, and (c) the base region, depends critically upon the depth of the junction below the exposed surface. It has been found that the use of a shallow junction is to be preferred, because of the associated improvement in blue response, and because the defects introduced during junction fabrication are also reduced in this design [14]. A further improvement in blue response obtains when the inevitable dopant graduation in the diffused layer is enhanced so that the accompanying field gradient accelerates minority carriers towards the junction field [14], and it is possible to predict analytically [26, 27] the improvement to be expected from a given dopant profile. The difficulty is that, in the diffusion process, independent control of the thickness of the doped layer, the dopant profile and average doping level is not possible, so that improvements which can be made in this way using conventional fabrication methods are limited.

The use of shallow junctions has to be accompanied by design features which minimize reflection of blue light from the cell surface if full advantage of the improvement is to be taken. This usually means that an antireflection coating is needed to match the refractive index of the covering material to that of silicon, and thin film TiO_2 is commonly used for this purpose. Ta_2O_5 has also been used [28], because of its tendency to form uniform amorphous layers (grain boundaries are detrimental to the optical transmission of the film), and more recently SiO and Si_3N_4 have been used [29] for matching to FEP teflon covers. Anti-reflection coatings have the disadvantage that their thickness has to be optimized for a single wavelength, and another technique for silicon is to etch the surface so that it becomes covered with small tetrahedra [30]. Reflected light is directed towards the surface of an adjacent tetrahedron, so that the reflectance of the surface is reduced uniformly across the spectrum. This is shown in Fig. 3, and a second advantage of the technique is clear from the diagram – the light path in the device is increased without increasing the distance from the junction at which carriers are generated.

Long wavelength photons tend to be absorbed deeper in the base region and consequently are only collected efficiently in relatively lightly doped, perfect material. The red response can be improved by increasing the base doping with distance from the junction so that, again, an electric field repels the carriers towards the junction [30–36]. Excessive doping will, however, cause increased recombination so there is a limit to improvements in this direction. Another method used to promote red response is to use good reflecting coatings on the back contact, so that absorption is facilitated without the need for unduly long diffusion lengths.

4.3.2. Series resistance

The fill factor of the device is determined by its resistance, decreasing by about 2.5% for each 0.1 Ω internal resistance [14]. The large series resistance of early cells was due to contact resistance, but this has been reduced by modern methods of contact fabrication. However, the move towards thin diffused layers in the cell has introduced another cause of high series resistance,

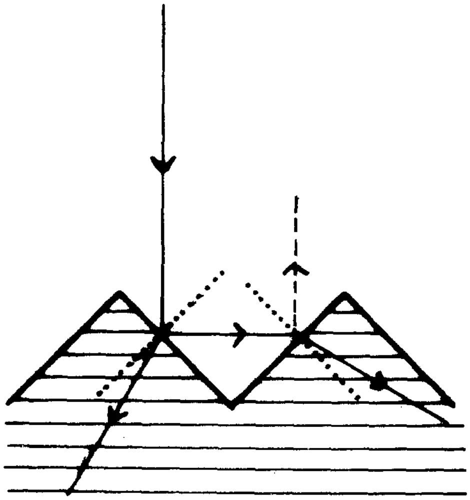


Figure 3 Reduced reflection due to the presence of tetrahedra on the surface of the cell, produced by etching (two-dimensional schematic illustration).

since the current flows laterally through this layer in order to reach the grid contact on the front of the device. Since the layer thickness can be as low as 0.5 μm, it clearly offers considerable resistance.

The area of the surface to be metallised and the thickness of the metal grid are both determined by the current which the contact must carry and the percentage transmission required. With these two parameters fixed, the series resistance of the diffused layer decreases as the contact area is broken down into an increasing number of fingers [14], so that the limit is the practical limit on the minimum finger width and spacing which can be achieved. A more detailed analysis for determining, for a given cell, the optimum front contact configuration for minimum series resistance has been published by Handy [37], taking into account the non-uniformity of performance across the diode area introduced because the surface is not completely covered by the top contact.

Passivated Ti(Pd)Ag contacts are almost universally used on production cells because these give low contact resistance and are compatible with conventional interconnect systems. However, the use of transparent electrodes covering the entire surface would remove the series resistance increase due to shallow junctions and in this case the cell resistance would be determined by its width and doping level, and any contact resistance. Transparent substoichiometric or doped oxide films can be deposited on glass at low temperatures by sputtering [38] and these films show low conductivity. However, these oxide materials do not generally form ohmic contacts on silicon so that high contact resistance precludes their use in this type of application.. Transparent metal contacts are similarly not useful because they have to be made very thin in order to be transparent, and they therefore offer high series resistance. Developments in the area of transparent contacts would, however, be extremely useful for silicon cell design, provided the problem of contact resistance can be overcome.

4.3.3. Maximized collection efficiency

The use of shallow junctions and graded doping to improve collection efficiency has already been discussed. Surface recombination can be reduced by passivation of the exposed surface by oxidation, and recombination in the junction region can be improved by using techniques of junction fabrication which do not damage the crystal too much, and which lead to an abrupt junction. Such techniques will be discussed later in the paper.

4.3.4. Maximized heat dissipation

Degradation of solar cell performance at elevated temperatures has already been discussed. One way of reducing the working temperature is to use a grid back contact which allows photons with energy less than the band-gap to pass through the device. A reduction in temperature from ~60° C to ~40° C by this method has been reported [39], and a corresponding improvement in V_{oc} has been obtained.

4.3.5. Optimized base resistance

It has been pointed out that, for an ideal junction, the base doping should be high, to allow maximum power output. However, in diffused junctions, the factors determining V_{oc} are usually the junction depth and the defects introduced into the junction region during processing. These effectively reduce V_{oc}, by reducing the effective barrier height, thus increasing J_o, and increased base doping does little to rectify the situation. Indeed, the power output of a practical device is often increased by increasing the base resistance, allowing longer diffusion lengths and hence better red response, and the limiting factor is usually the need to keep the series resistance (rather than the leakage current) acceptably low.

4.3.6. Optimized base width

The useful base region is determined by the absorption characteristics of the material and the diffusion length for minority carriers in the region. If the base width greatly exceeds the diffusion length, then unnecessary series resistance is introduced.

4.3.7. n-on-p or p-on-n?

One other design feature which can usefully be discussed here is the conductivity type of the base and diffused regions. In the first production of solar cells (~ 1958) n-type bases were used, and a surface p-layer was diffused into them. This was because the minority carrier mobility is generally higher for electrons than for holes, and the highest minority carrier mobility was required in the region of highest absorption ← the front of the cell. The product was changed to n-on-p when it became clear that this configuration withstood the incident high energy radiation encountered in space better than its predecessor, but the efficiency of these devices was less than the equivalent p-on-n structure [1]. For terrestrial applications, the latter could usefully be reinvestigated, in the light of all the other factors which have been introduced since to improve efficiency.

4.4. Mode of operation of solar cells

The power density available from an array of solar cells could, in principle, be increased by focusing the incident radiation to increase J_L. However, there is a maximum in the curve of power density versus illumination level, which for silicon occurs at quite low levels of illumination. The reasons for this are:

(1) the temperature of the cell rises, reducing V_{oc};

(2) at high carrier concentrations complex recombination processes occur, reducing J_{sc};

(3) the power lost in the surface layer increases as the current increases ($\propto J^2R$).

The simple diffused junction solar cell can be designed to reduce effects (2) and (3) by using lightly doped material [40], large contact area and deep junctions [41]. Of course, this reduces their low intensity efficiency, so that their sensitivity of output to conditions of reduced solar intensity would be very much increased.

A more complex design, intended to allow high temperature operation, has been the use of stacks of junctions illuminated by light incident in the junction plane [42]. In this device the effect of series resistance in the thin layer is removed, and diffusion lengths need only be very small. However, its potential has not been realized in practice because of the serious surface recombination problem, and because a gradient in potential occurs along the junction, leading to circulating currents which reduce efficiency [43].

As pointed out in Section 4.1.3, there are also problems associated with the collector system itself. First, the collector system would have to track the sun, and secondly, concentration is relatively ineffective in areas which receive a high percentage of the total insolation as diffuse rather than direct radiation. Further, heat dissipation systems would be needed to keep the cells reasonably cool, and while adequate systems can be designed for this purpose [44], with the extracted heat usefully absorbed and used in a collection system, the fact is that the best collector design changes with the installation environment (wind speed, % direct radiation, ambient temperature etc). These design variables lead to changes in the operating condition of cells (i.e. temperature and illumination level) which would mean that the cell design would need to be optimized differently for each environment. GaAs for use with concentrators could be cost-competitive [41], but would require substantial development of fabrication methods to reach large volume production, and this move would not remove the serious disadvantages of concentrator systems with respect to maintenance, deterioration of cell encapsulation with long-term exposure to intense light and long-term deterioration of the concentrator surfaces due to atmospheric and environmental factors.

The third and most likely approach to reducing the cost/watt of solar energy is to reduce production costs for standard silicon cells. The following sections will outline the possibilities here.

5. Substrate fabrication

Conventional diffused p-n junctions use single crystal silicon, pulled from the melt by the Czochralski technique, which yields high quality crystals (often dislocation free) having dimensions typically 60 cm long x 7.5 cm diameter, grown at about 10 cm h^{-1}. This is an expensive process in terms of the equipment cost, the large energy consumption during growth and the lengthly and wasteful processing needed to prepare thin polished substrates from the crystals grown. Nevertheless it appears that, if automated control of growth and other equipment design features can be upgraded to produce 15 cm diameter crystals grown at 17 cm h^{-1} and having reasonable quality, the process could meet cost criteria for solar cells [45]. This process improvement appears to be within the bounds of possibility.

More economical processes are, however, under consideration. One of these, edge-defined film-fed growth (EFG), is a modification of the Czochralski technique in which the melt is drawn into ribbon shape by capillary rise through a partially immersed die in the melt [46]. This technique offers the possibility of achieving very high temperature gradients at the growing interface, and hence should give good crystal/melt interface stability. Normally dissipation of the latent heat of crystallization through the grown crystal provides a limit to the growth rate. However, for crystals with a large area:volume ratio (e.g. ribbon), heat dissipation by radiation to the surroundings is very efficient, and fairly high growth rates can be used [47]. The actual rate is largely determined by the need to achieve planar isotherms across the upper surface of the die, and typical rates for silicon are 1 to 3 cm min^{-1} [48]. 0.8 mm x 25 mm x 20 m ribbons, wound on 1 m diameter reels, have been produced using the technique.

The major difficulty at the moment is contamination of the crystals by SiC, arising from chemical reaction of the melt with the carbon die. Although SiC in silicon is not electrically active, problems arise because of associated crystallographic defects. There are also difficulties due to the thermal instability accompanying this inherently small volume crystallization, which makes control during the early stages of seeding and broadening the ribbon difficult to achieve.

EFG ribbons have produced cells having acceptable efficiency, despite the contamination problem [49]. It appears that these give shallower diffusion depths than conventional substrates for the same diffusion conditions, and thus the cells made from EFG tend to show good blue response. The precise relationship between defect density (and type) and solar cell performance is not yet established, but there is no reason to doubt that EFG will be able to produce material with sufficient quality for solar cell application. The limit to its usefulness is likely to be economic, with production targets of 15 cm x 0.01 cm for the cross-sectioned area of ribbons, pulled 15 at a time, needed for sufficiently low cost devices [45]. This is a very severe specification and it remains to be seen whether it can be achieved, and if so, in what time.

With the discovery that polycrystalline substrates are probably useful for solar cell applications, attention is increasingly turning to low cost methods for their fabrication. Sputtering [50] or evaporating [51] amorphous or small grain films have both been suggested, to be followed by post-deposition recrystallization. The use of laser heating (Nd:YAG) [52] to crystallize 6 to 11 μm thick films of amorphous silicon has produced 25 μm grain size, but the use of laser radiation (which is produced with only about 2% efficiency) appears to be wasteful in terms of the energy balance of fabrication and device operation. Thermal recrystallization of small (1 μm) grain size films has produced an improvement in size of a factor of 100 [53] and it is not unreasonable to suppose that 100 μm grain size is acceptable for solar cell operation, although long annealing times are necessary to achieve this, making the economics of such a process unfavourable. More highly controlled processes involving the passage of a molten zone across polycrystalline films are currently under investigation [54], and although these present difficulties in controlling the zone shape and stability, refinement of the techniques is expected to produce improved results.

The photovoltaic effect in amorphous silicon diodes has recently been demonstrated [55]. Amorphous layers can be made by the glow discharge dissociation of silane doped with diborane or phosphene as appropriate, and the junction can be formed by successive depositions of appropriately doped material. Amorphous films allow cheap processing to be used, without the introduction of difficulties associated with grain boundaries, but many problems remain to be solved before these can give devices of acceptable efficiency.

Returning now to polycrystalline material, epitaxial deposition can be used to form silicon layers on metals, and the grain size of these films is likely to exceed that of evaporated or sputtered films. The most obvious method to use is chemical vapour deposition [56, 57] since the technique (using the decomposition of SiH_4, or the reduction of $SiCl_4$, or SiH_2Cl_2) has been widely used for homoepitaxy, and for the deposition of silicon on insulating substrates such as sapphire and spinel [21, 58, 59]. Major difficulties remain, however, in the choice of substrates, since:

(1) silicon reacts with most metals, even at the relatively low temperatures needed for deposition from the vapour, and the layer of silicon–metal (or SiC for carbon substrates) formed at the interface is usually insulating;

(2) metals generally have high thermal expansion coefficients compared with that of silicon, so that the junction quality might be affected adversely. In fact, the formation of a graded silicon–metal layer between the film and the substrate might help in this respect;

(3) CVD films are very sensitive to the preparation of the substrate surface, and the need for careful substrate preparation might well be a serious adverse factor, since fabrication costs will be increased.

Two-rate deposition has been used to reduce the contamination of CVD silicon by insulating substrates [60] and this technique might have application for deposition on metals. Fang [61] has suggested that deposition at about 800° C on titanium-passivated stainless steel can produce acceptable silicon films, but it is still true that the selection of a suitable conducting substrate remains the principal factor limiting the development of CVD silicon cells.

The use of carbon substrates for the deposition of silicon from the melt has lead to devices with 5% efficiency, despite the problem of SiC contamination [62]. This dipping process can be designed as a continuous operation, and offers a good deal of promise. A substrate which does not react with silicon to form an insulating layer would improve the process, and there remains the possibility of reducing the temperature of deposition (and hence the contamination from the substrate) by depositing silicon from a metal solution. The seeded growth of silicon from solutions in tin was reported as early as 1953 [63], and has been suggested recently as the basis of a production process [2].

More speculative substrate fabrication techniques, such as hot rolling and subsequent stress-anneal recrystallization, have been suggested in the past [64] but not developed until recently [2]. It is probable that epitaxial films on conducting substrates could be used (perhaps with post-deposition recrystallization) to produce cells having an acceptable cost:efficiency ratio, but the deciding factor in their future commercial importance will be the time taken to develop the fabrication techniques to the stage where these films compete seriously with single crystal (Czochralski or EFG) slices. The development of EFG will undoubtedly continue to receive attention, and again, its competition with bulk crystal technology will be determined by the rate at which cost:efficiency targets can be reached rather than the ultimate performance achievable.

6. Junction fabrication techniques

As we have seen, the conventional diffused junction has some important drawbacks which have already been mentioned. These are that the defect content of the diffused layer is high, the junction tends to be non-abrupt, and the doping profile is not easily varied without also varying the layer depth. For these reasons, attention has turned recently to other techniques of forming p–n junctions in silicon.

One method of introducing a controlled thickness dopant layer of required concentration is by the use of ion implantation, achieved by the incidence on the base crystal of an accelerated ion beam of the required dopant species [65]. Control of the dopant profile is achieved independently of the quality of the host lattice, whereas the diffusion of dopant by more conventional methods is strongly influenced by host lattice perfection. The technique offers additional advantages over diffusion: lateral definition of the doped region is easily achieved when conventional photolithography is used, and further, the ultimate concentration of dopant is not restricted by solid-solubility limits, since implantation is a rapid, non-equilibrium process.

Various semi-empirical tabulations are available for relating the depth of penetration of a given dopant in a given host to the ion-beam energy, offering better control than is obtainable with diffusion doping. Accelerating voltages 10 to 1000 kV are typically used to produce layers within 2 μm of the surface and, if desired, buried dopant layers are possible by the technique.

As with diffusion, the implanted dopant process produces lattice damage. At low dopant concentrations, this damage tends to be localized (particularly for light ions) and readily anneals out at about 250° C. At higher dopant levels, however, extensive damage is done, particularly in compounds having highly directional bonds, and covalent materials (Ge, Si, GaAs) become disordered under heavy bombardment, forming amorphous surface layers.

Recrystallization of these disordered regions is possible, often at fairly low temperatures [66], although this depends to some extent on the energy and density of bombarding ions, their mass, and the way in which they enter the lattice. Much work is needed on optimizing post-implantation annealing treatment, but generally the induced damage can be reduced to an acceptable degree (comparable with diffusion-induced damage). There are, of course, limitations on the maximum annealing temperature which can be used, partly due to cost, and partly due to the need to avoid diffusion of the implanted dopant. Despite these limitations, shallow junction solar cells having improved blue response and acceptably low leakage current and sheet resistance have been made by this technique [39].

A third technique for junction formation is to use the epitaxial deposition of suitably doped silicon onto single crystal or polycrystalline substrates. Relatively little work has been done on deposition of silicon on silicon from the melt or solution, but deposition on silicon by chemical vapour deposition has been more widely studied, and used for polycrystalline substrates with some success [24]. It appears that CVD in this case is to be preferred to conventional diffusion because carrier generation-recombination at the grain boundaries in the substrate and film seems to be suppressed to some extent. The junction quality is good, and the control and/or grading of dopant profile is facilitated by the technique. There appear to be no major disadvantages to the use of CVD to form junctions on silicon except perhaps the requirement of a good substrate surface, and the extent to which the technique is used in practice is likely to be determined by the economics of the process.

Epitaxy from the solid phase of antimony doped silicon on silicon has been reported recently [67], by using solid state diffusion of the doped material through a buffer layer of Pd_2Si. This technique is at a very early stage of development, and its commercial possibilities are uncertain, but it is included here for completeness.

7. Silicon Schottky barriers

Up to this point, only silicon p–n junctions have been considered in detail. The necessary potential discontinuity for photocarrier separation can, of course, be achieved by depositing a thin metal film in a silicon substrate, and this type of device requires relatively fewer processing steps than the p–n junction type. The limiting factor has so far been that the small barrier heights obtainable led to low efficiency. It has recently become apparent that there are a number of ways in which the barrier height can be increased, and a number of acceptably efficient devices have been made. The use of an interfacial oxide layer between the metal and the semiconductor has allowed an appreciable improvement in cells of Au:n-Si [68, 69] and Al:p-Si [70]. Theoretical understanding of the effect of oxide layer thickness and of interfacial states at the semiconductor-oxide surface is well advanced [71–73] so that device design can be optimized by using modelling. The Hf:n-Si system is characterized by a large barrier height, and has been used successfully in devices [74]. The same authors have demonstrated the use of ion implantation to reduce the surface doping in silicon prior to metallization, which is another technique for increasing the junction barrier height.

A reduction in the sheet resistance of the metal layer can be achieved using double layers, with Cr to give a high potential barrier, followed by Cu, to enhance the conductivity for a given metal thickness [75]. The temperature characteristics of this double-layered device have been studied both theoretically and experimentally [76], and are well understood. The optimization of metal layer area with respect to the cell area offers the possibility of further improvements in efficiency [77], and metal/Si systems seem to merit extensive further developments for use in low cost solar cell production.

A Schottky barrier also forms at a semiconduction/electrolyte interface, and this has led to speculation about the possibilities of electrolytic cells. A number of compound semiconductor anodes have been investigated [78, 79] for this purpose and recently, a silicon electrolytic cell has been reported [80]. These cells have the obvious advantages that the junction is abrupt, formed without any processing, and free therefore from process-induced defects. Unfortunately, electrolytic dissolution or passivation of the anode occurs for most semiconductor/electrolyte systems, so that the lifetime of such a cell will be low, unless this battery action can be avoided. At the present time, only n-type rutile [81] has been shown to be completely stable in anodic applications, and this material ($E_g \sim 3\,\mathrm{eV}$) matches the solar spectrum inefficiently. The use of electrolytic cells in characterising the photoresponse of cells at each stage in manufacture has been reported recently by Fabre *et al.* [82, 83] and this is probably the most important photovoltaic application of semiconductor/electrolyte systems.

8. Conclusions

The development of cheap processing for the preparation of thin silicon substrates is the area of solar cell technology which is currently receiving most attention. This reflects the commitment of the electronics industry all over the world to silicon, and it is unlikely that this inertia will be overcome in favour of some new material, unless a substantial improvement over silicon can be demonstrated. At the present time, with the pressure on companies to move into the terrestrial solar cell market on a large scale within the next ten years, it seems unlikely that any other material will gain precedence.

Cheap fabrication may well involve a move towards polycrystalline silicon, but here again, if current technology is to be superceded, a substantial improvement in the resulting product will have to be demonstrated. There is still a reasonable probability that Czochralski crystal pulling will be used to make the next generation of silicon solar cells.

Outside the US, the economic criteria for large-scale application of solar cells are less stringent, and it is probable that these could be met using currently developed technology, with cost reduction achieved by optimizing cell design. This might well involve improved methods of junction fabrication to replace the diffusion process.

The research areas which are going to be of greatest importance to solar cell technology over the next few years are likely to be:

(a) deposition of 100 μm thick silicon films on conducting substrates, and their post-deposition recrystallization;

(b) transparent, conducting electrodes forming low resistance contacts on silicon;

(c) epitaxy and ion implantation for junction formation;

(d) theoretical and experimental evaluation of the effect of grain boundaries and process-induced defects on solar cell performance;

(e) optimization of the design of production-line solar cells, within the limits imposed on crystal quality and particularly junction perfection by the production process, and the economic limits relevant to large scale application;

(f) upgrading of EFG and Czochralski pulling to produce cells of optimum cost: efficiency.

There seems to be little advantage in moving to concentrated solar radiation, particularly in view of doubts about the long-term performance of such systems. Similarly, Schottky barrier devices are unlikely to prove sufficiently superior to normal p–n junction devices to merit a move in this direction. Finally, detailed economic study of the use of solar cells outside the US, and in particular in the developing countries, will prove invaluable in establishing the cost-criteria which in turn determine the research priorities which should be observed by those involved in solar energy utilization in these areas.

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